FIG. 1(a)

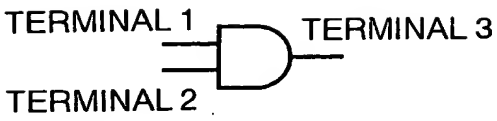


FIG. 1(b)

INPUT PIN	OUTPUT PIN	RISE/FALL OF INPUT	RISE/FALL OF OUTPUT	DELAY TIME (ns)
TERMINAL 1	TERMINAL 3	rise	rise	1
TERMINAL 1	TERMINAL 3	rise	fall	2
TERMINAL 1	TERMINAL 3	fall	rise	3
TERMINAL 1	TERMINAL 3	fall	fall	4
TERMINAL 2	TERMINAL 3	rise	rise	5
TERMINAL 2	TERMINAL 3	rise	fall	6
TERMINAL 2	TERMINAL 3	fall	rise	7
TERMINAL 2	TERMINAL 3	fall	fall	8

FIG. 1(c)

TERMINAL 2 / TERMINAL 1	0	1
0	0	0
1	0	1

FIG. 2

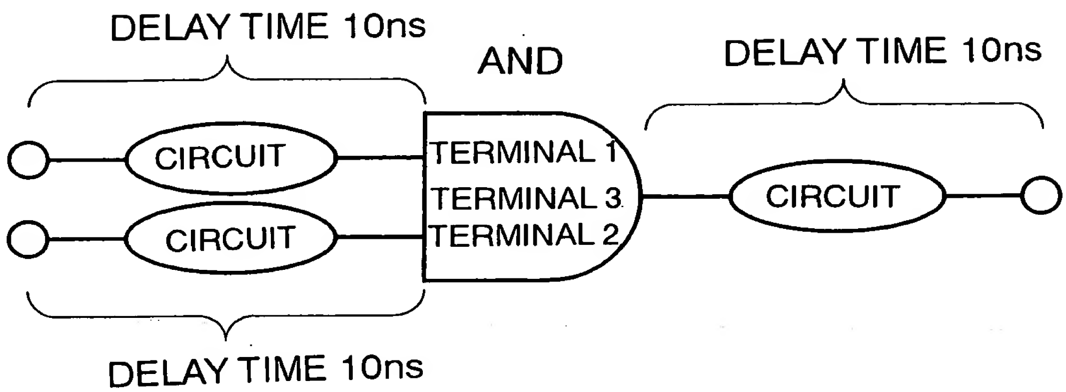


FIG. 3

RISE/FALL OF INPUT	BOTH INPUTS RISE	Rise/fall	BOTH INPUTS FALL
INPUT 1			
INPUT 2			
OUTPUT			
DELAY CAUSED BY: INPUT	INPUT RISING LATER	NONE	INPUT FALLING EARLIER

FIG. 4

OUTPUT	SELECTED INPUT
Rise	INPUT RISING LATER
Fall	INPUT FALLING EARLIER

FIG. 5

INPUT PIN	OUTPUT PIN	RISE/FALL OF INPUT	RISE/FALL OF OUTPUT	DELAY TIME (ns)	
TERMINAL 1	TERMINAL 3	rise	rise	1	
TERMINAL 1	TERMINAL 3	rise	fall	2	
TERMINAL 1	TERMINAL 3	fall	rise	3	OUTPUT RISES
TERMINAL 1	TERMINAL 3	fall	fall	4	
TERMINAL 2	TERMINAL 3	rise	rise	5	
TERMINAL 2	TERMINAL 3	rise	fall	6	OUTPUT FALLS
TERMINAL 2	TERMINAL 3	fall	rise	7	
TERMINAL 2	TERMINAL 3	fall	fall	8	

FIG. 6

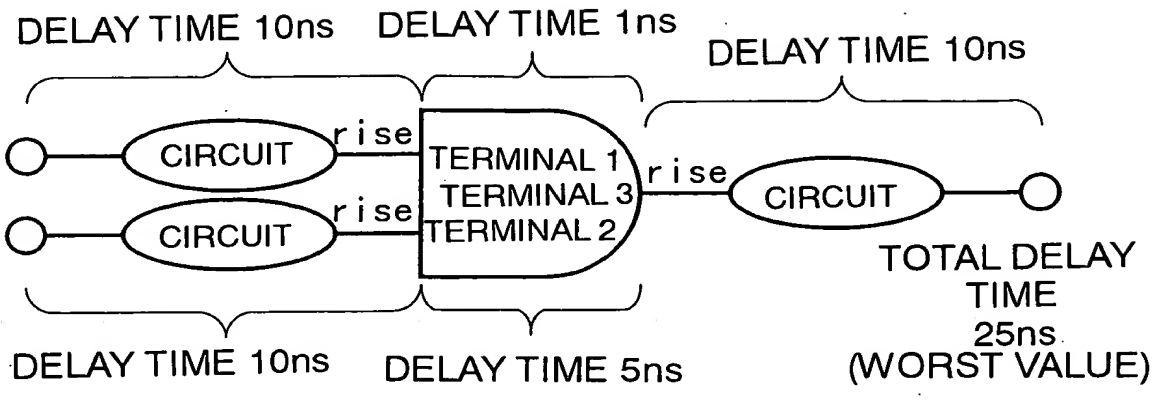
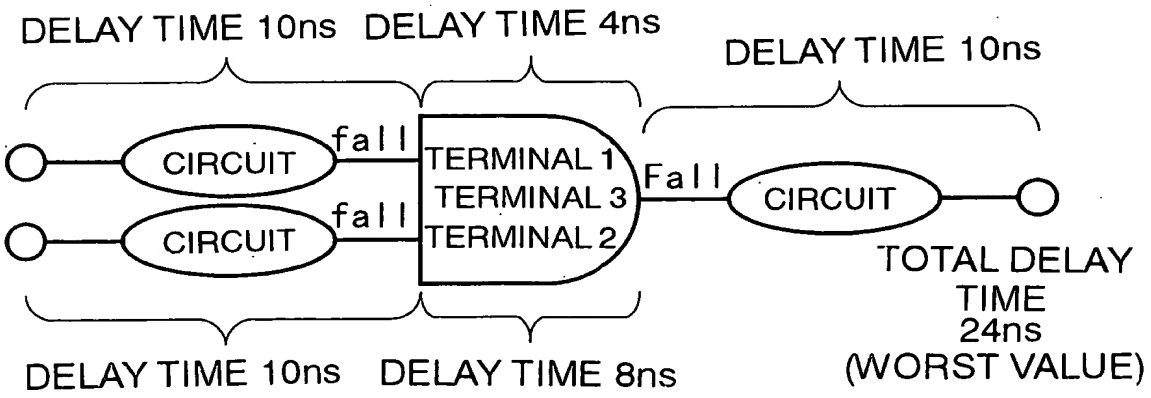

DELAY TIME 10ns
DELAY TIME 1ns
DELAY TIME 10ns
CIRCUIT
rise
CIRCUIT
rise
TERMINAL 1
TERMINAL 3
TERMINAL 2
rise
CIRCUIT
TOTAL DELAY TIME 25ns (WORST VALUE)
DELAY TIME 10ns
DELAY TIME 5ns

FIG. 7


DELAY TIME 10ns
DELAY TIME 4ns
DELAY TIME 10ns
CIRCUIT
fall
CIRCUIT
fall
TERMINAL 1
TERMINAL 3
TERMINAL 2
Fall
CIRCUIT
TOTAL DELAY TIME 24ns (WORST VALUE)
DELAY TIME 10ns
DELAY TIME 8ns